REMARKS

Reconsideration of the above-indicated patent application, as amended, is respectfully requested. The present amendment is responsive to the Final Office Action mailed December 12, 2003. Claims 1-20 have been rejected. Accordingly, claim amendments, new claims and supporting remarks are hereby presented that particularly point out and distinctly claim the subject matter that applicant regards as the invention. No new matter has been added.

THE INVENTION

The present invention had been described in detail in the response to the previous action. In the Final Action, the Examiner has repeated the previous rejections as applied to claims 2-7 and 8-20, and has tendered a new grounds of rejection as applied to claims 1-8. In connection with the response to the previous action, the Examiner has stated that, "the features upon which applicant relies, (i.e. repeatedly executing a single instruction without refetching) are not recited in the rejected claims(s)." The previous amendment revised the claims from "at least one associated instruction" to "an associated instruction." In this way, it was believed that the claims were limited to a single instruction. However, the Examiner had not acknowledged this distinction, and the present claims have now been amended to explicitly recite "a single instruction." Support from this amendment can be found from the entire disclosure, e.g. page 12, line 21. Therefore, it respectfully requested that this distinction now be given the proper weight and that the claims now be considered as distinguishing over the prior art.

THE REJECTIONS UNDER 35 U.S.C. §102

Claims 1 and 8 had been rejected under Section 102(b) as allegedly being anticipated by Zolnowski et al. (U.S. Pat. No. 4,566,063). This rejection is respectfully traversed, particularly as applied to the amended claims as presented herewith.

Zolnowski et al. is directed to a data processing system that can repeat the execution of instruction loops with minimal instruction fetches. This system is a "pipelined" system in which a number of instructions are provided in an "instruction stream." The instruction pipeline is filled up using prefetched instructions. However, there is no discussion in Zolnowski et al., (either in the cited portion at col.11, line 58 et seq., or elsewhere in the reference) of a system for fetching a single instruction and repeatedly executing that instruction without refetching, as is the subject of the present claims. Reconsideration and withdrawal of this grounds of rejection is therefore respectfully requested.

Claims 1-7 had been rejected under Section 102(b) as allegedly being anticipated by Shridhar, et al. (U.S. Pat. No. 5,727,194). This rejection is once again respectfully traversed, particularly as applied to the amended claims as presented herewith.

As was shown previously, Shridhar et al. is directed to a system including a repeat bit execution of repeat loops. It is once again quite clear from inspection that Shridhar et al. is a "pipelined" loop system in which a sequence of instructions is repeatedly fetched, decoded and executed. However, it is once again respectfully submitted that there is no discussion in Shridhar et al. of a system for fetching a single instruction and repeatedly executing that instruction without refetching, as is the subject of the present claims. And further, the Examiner had considered the previous amendments and arguments to be non-persuasive on the basis that the

claims had not used the precise expression "single instruction." Now that this language is explicitly recited in this limitation, it is respectfully submitted that this basis for continued rejection of the claim is overcome, and that the present amendments and arguments, along with previous supporting arguments, should now be sufficient to be deemed persuasive. As such, reconsideration and withdrawal of this grounds of rejection is once again respectfully requested.

Claims 9-20 had been rejected under Section 102(b) as allegedly being anticipated by Kiuchi et al. (U.S. Pat. No. 5,579,493). This rejection is once again respectfully traversed, particularly as applied to the amended claims as presented herewith.
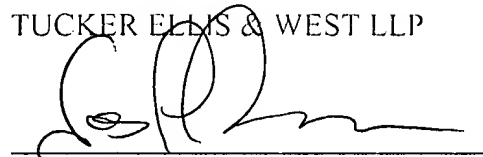
As was shown previously, Kiuchi et al. discloses a system that uses a loop buffer for storing instructions that are repeatedly executed, in order to decrease power consumption on the data processor. However, it is once again respectfully submitted that there is no discussion in Kiuchi et al. of a system for fetching a single instruction and repeatedly executing that instruction without refetching, as is the subject of the present claims. And as discussed above in connection with the Shridhar et al. reference, now that the "single instruction" language is explicitly recited in the claims, it is respectfully submitted that this basis for continued rejection of the claim is overcome, and that the present amendments and arguments, along with previous supporting arguments, should now be sufficient to be deemed persuasive. As such, reconsideration and withdrawal of this grounds of rejection is once again respectfully requested.

In view of the foregoing it is respectfully submitted that the present claims, as currently amended, distinguish over the prior art. A notice to that effect is earnestly solicited. If the

Examiner believes there are any further matters, which need to be discussed in order to expedite

the prosecution of the present application, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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